

Applic. No.: 10/075,539

Amdt. Dated May 16, 2005

Reply to Office action of February 18, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended). A memory configuration, comprising:

at least two semiconductor memory modules, including a first semiconductor memory module and a second semiconductor memory module, controlled by internal clock signals, said two semiconductor memory modules output or receive data only on one of a rising edge and a falling edge;

an interface device for receiving an external clock signal and the data on a rising edge and a directly succeeding falling edge of the external clock signal or ~~outputs~~ outputting the data between the rising edge and the directly succeeding falling edge of the external clock signal; and

a conversion device connected between said interface device and said two semiconductor memory modules to route the data for outputting or reception;

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the external clock signal being fed to said interface device,  
and said conversion device generating complementary clock  
signals, of which one of the complementary clock signals being  
fed to said first semiconductor memory module and another of  
the complementary clock signals being fed to said second  
semiconductor memory module;

said conversion device having a command decoder for detecting  
a command for receiving data, the command for receiving data  
containing at least two signal pulses present on the rising  
edge of the external clock signal, and the command for  
receiving data being forwarded to said first semiconductor  
memory module in a manner delayed by 3 1/2 clock periods of the  
external clock signal and being forwarded to said second  
semiconductor memory module in a manner delayed by three clock  
periods of the external clock signal;

said command decoder detecting a command for outputting data,  
the command for outputting data containing two signal pulses  
present on the rising edge of the external clock signal, and  
the command for outputting data being forwarded to said first  
semiconductor memory module in a manner delayed at most by one  
clock cycle of the external clock signal and being forwarded  
to said second semiconductor memory module in a manner delayed  
at most by 1 1/2 clock periods of the external clock signal.

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Claim 2 (cancelled).

Claim 3 (currently amended). The memory configuration according to claim [[2]] 1, wherein said conversion device has a delay locked loop with an input side receiving the external clock signal and an output side outputting the complementary clock signals functioning as the internal clock signals, said delay locked loop connected to said interface device.

Claims 4-5 (cancelled).

Claim 6 (currently amended). The memory configuration according to claim [[4]] 1, wherein the command for receiving data contains the two signal pulses that each have a low level and are centered with respect to two rising edges of the external clock signal that are separated by two clock periods.

Claim 7 (currently amended). The memory configuration according to claim [[2]] 1, wherein:

said first semiconductor memory module has a data signal terminal;

said second semiconductor memory module has a data signal terminal; and

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said conversion device has a changeover switch with a first terminal connected to said interface device, a second terminal connected to said data signal terminal of said first semiconductor memory module, and a third terminal connected to said data signal terminal of said second semiconductor memory module, said changeover switch able to switch over between said second terminal and said third terminal, and ~~in~~ that a driving of said changeover switch can be controlled in a manner dependent on each edge change of the external clock signal.

Claim 8 (original). The memory configuration according to claim 7, wherein

said interface device has a data signal terminal; and

a first data value to be output or input at said first semiconductor memory module and a second data value to be output or input at said second semiconductor memory module are alternately present at said data signal terminal of said interface device after every half clock period of the external clock signal.

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Claim 9 (original). The memory configuration according to claim 1, wherein said conversion device contains a signal generator for generating a clock signal whose edges are oriented to edges of a data signal during a data outputting and which has edges which are oriented to a binary signal level of the data signal during a data inputting.

Claim 10 (original). The memory configuration according to claim 1, wherein said conversion device has at least two further memory modules for storing a respective further bit of a data word, one of said further memory modules is connected in parallel with said first semiconductor memory module and another of said further memory modules is connected in parallel with said second semiconductor memory module.

Claim 11 (currently amended). The memory configuration according to claim [[5]] 1, wherein the command for outputting data contains the two signal pulses that each have a low level and are centered with respect to two rising edges of the external clock signal which are separated by two clock periods.